PROGRAM DEBUG METHOD AND APPARATUS

ABSTRACT

5   The present invention provides for an apparatus
employed to debug a program operating in a supplemental
processor when the processor's registers are not readable
directly by the debugging operation of a main processor. A
program operating in main memory halts due to operational
10   errors. The program code lines save to a cache. In the
main processor, a pool of memory is reserved. A copy of the
data from the nominally inaccessible supplementary
processor registers also transfers to the reserved storage
area for processing of the program needing debugging. After
15   the program debugging is complete, a copy of the contents
of the memory pool is restored to the memory of the target
supplemental processor. A copy of the local store register
state and remaining local store data returns to main
memory.